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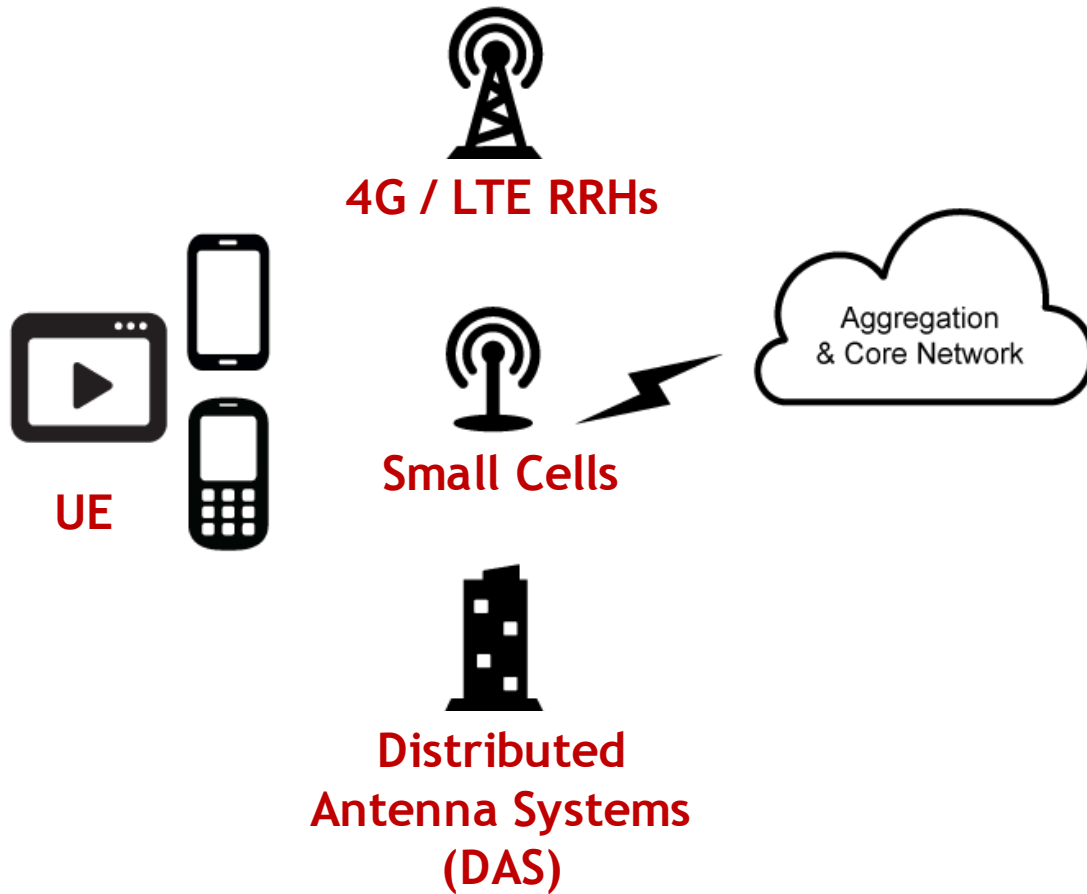


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Simplifying Radio Access
Network Clocking Using
Proven DSPLL
Technology

Carriers Deploying Low Cost, Low Power RAN Nodes

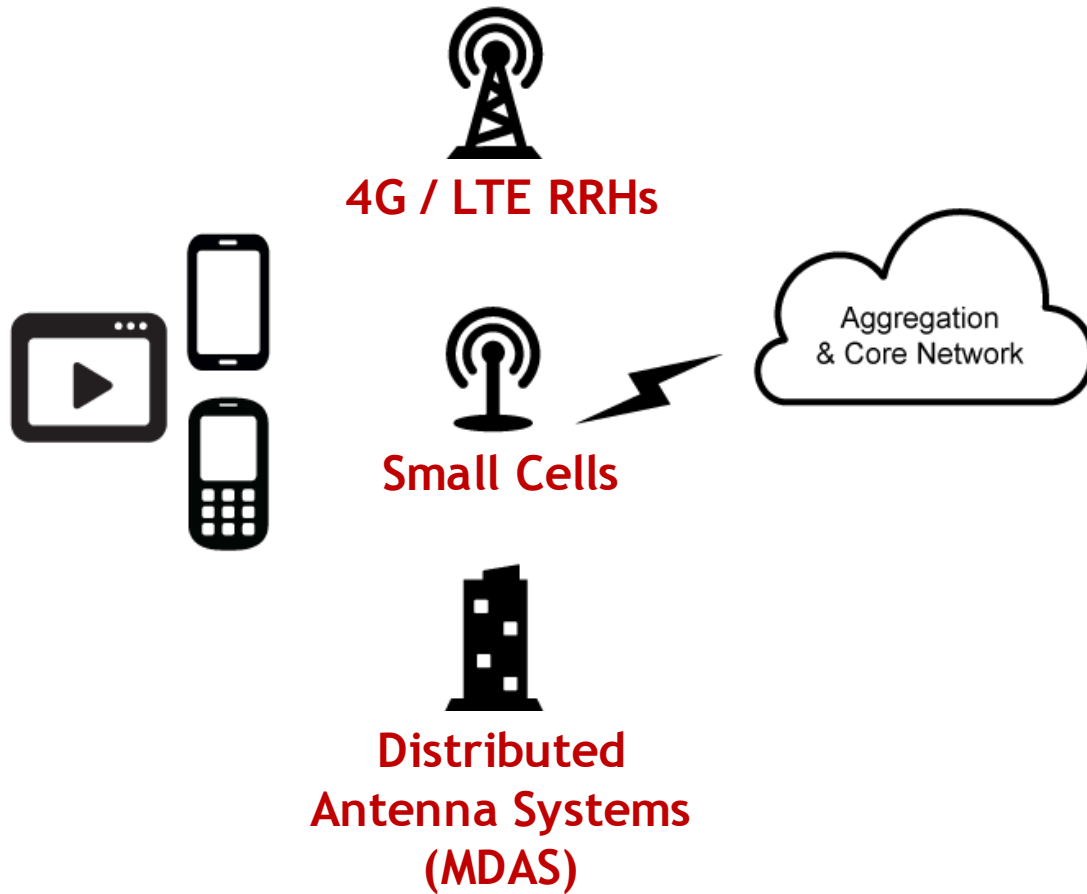
Radio Access Networks (RAN)



- Wireless service providers under pressure to expand network capacity and coverage to support bandwidth-intensive services.
- Operators deploying a heterogeneous network (HetNet) of small, low-power Radio Access Network (RAN) nodes:
 - **Remote Radio Heads (RRHs)** in 4G/LTE base stations increase network coverage and capacity.
 - **Small cells** improve coverage in dead spots, and offload wireless data to fixed wireline IP networks closer to the end user.
 - **Distributed Antenna Systems (MDAS)** complement RRHs and small cells to extend network coverage and ensure seamless “five-bar” service in office parks, hotels and public areas like arenas and concert facilities.

RAN Nodes are Optimized for Size, Power, and Performance

Radio Access Networks (RAN)



- RAN designs are space constrained, relatively inexpensive compared to other networking equipment, and may be deployed in non-temperature controlled locations.
- They must be optimized for size, power, performance, and cost.
- This ebook covers a **proven timing technology** that...
 - ✓ **reduces current timing BOM footprint 66%**
 - ✓ **reduces power consumption by 30%**
 - ✓ **increases design flexibility**
 - ✓ **reduces system costs**

RAN Timing Requirements Diverse and Demanding

- Despite the fact that RAN devices must be small, affordable, and reliable in outside elements, the **RF timing specifications remain stringent due to wireless phase noise requirements.**
- **RAN devices require an increasing mix of frequencies to support system-level functions,** some of which are shown on the next page.
- These combined requirements **drive increased complexity, power consumption, and footprint** because **traditional timing solutions are inflexible, power hungry, and require multiple discrete components.**

RAN System Requirements Drive Timing Complexity

- RF timing specifications remain very stringent. An increasing mix of frequencies is required to support system-level functions without sacrificing performance.

Application	Example Frequencies	
4G/LTE data converters	- 30.72 MHz - 61.44 MHz - 122.88 MHz	- 245.76 MHz - 491.52 MHz - 983.04 MHz
RF transceivers	- 25 MHz - 40 MHz	- 100 MHz
Ethernet PHYs	- 25 MHz - 125 MHz	- 156.25 MHz - 322.265625 MHz
System clocks	- 25 MHz	- 66.666 MHz

Common Timing Reference Frequencies Used in RAN Equipment

Introduction to DSPLL vs. Current Timing Architectures

- Traditional RAN designs use **cascaded, two-stage phase-lock loop (PLL)** technology for high-performance, low phase noise clock synthesis.
- Cascaded, two-stage PLLs **provide excellent phase noise performance**, but **suffer from limited frequency flexibility, high power, sensitivity to noise and vibration, and a large, discrete footprint including external VCXOs and loop filters.**

RAN designs need smaller, more flexible, better timing solutions to meet today's requirements.

Introduction to DSPLL vs. Current Timing Architectures

DSPLL timing technology addresses RAN's timing needs.

- **DSPLL** addresses these challenges in a **single IC that offers low phase noise, greater frequency flexibility, lower power, and better immunity to noise and vibration effects** than current solutions.
- While this new technology may sound too good to be true...

DSPLL is Already Widely Deployed in Telecom Apps

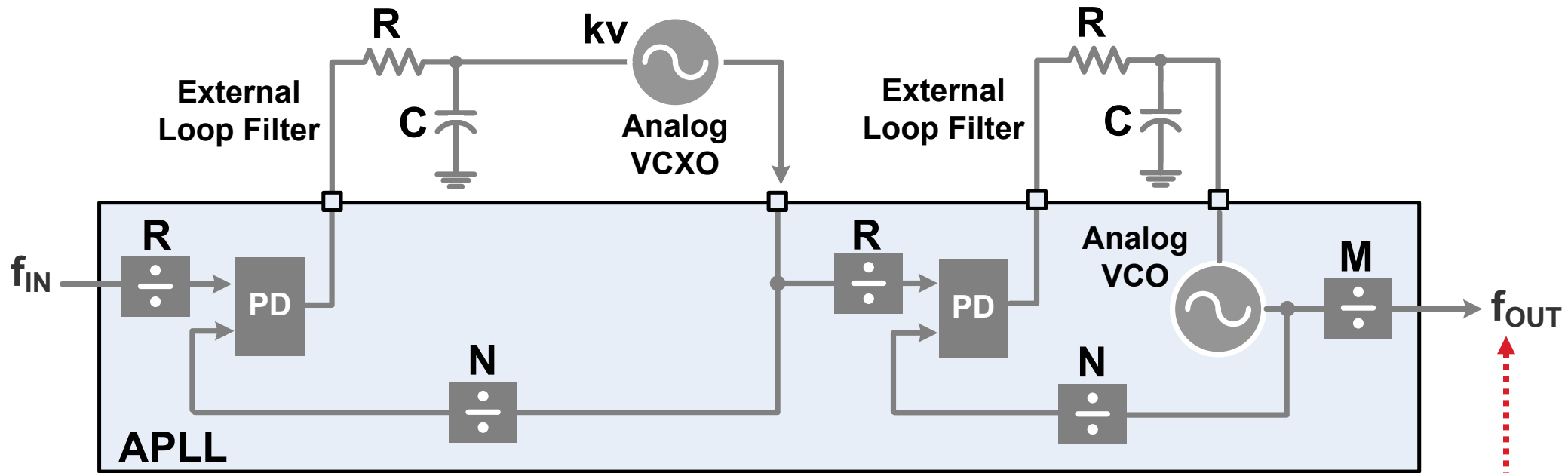
- ... in reality DSPLL has **already been widely adopted and deployed** in demanding telecommunications and networking applications within core, metro and access equipment, including cutting-edge 100G/400G SerDes clocking applications.

**>50 Million DSPLL-enabled Nodes Already Deployed
in High-Performance, Demanding Telecom and
Networking Applications**

**Hundreds of Millions
of Reliable Operating Hours**

Legacy, Cascaded, Two-Stage PLL Architecture

- A cascaded, two-stage PLL is the traditional analog architecture for RAN designs.
- It delivers low phase noise but only for a restricted set of output frequencies
- The output frequency must be integer-related to its input frequency

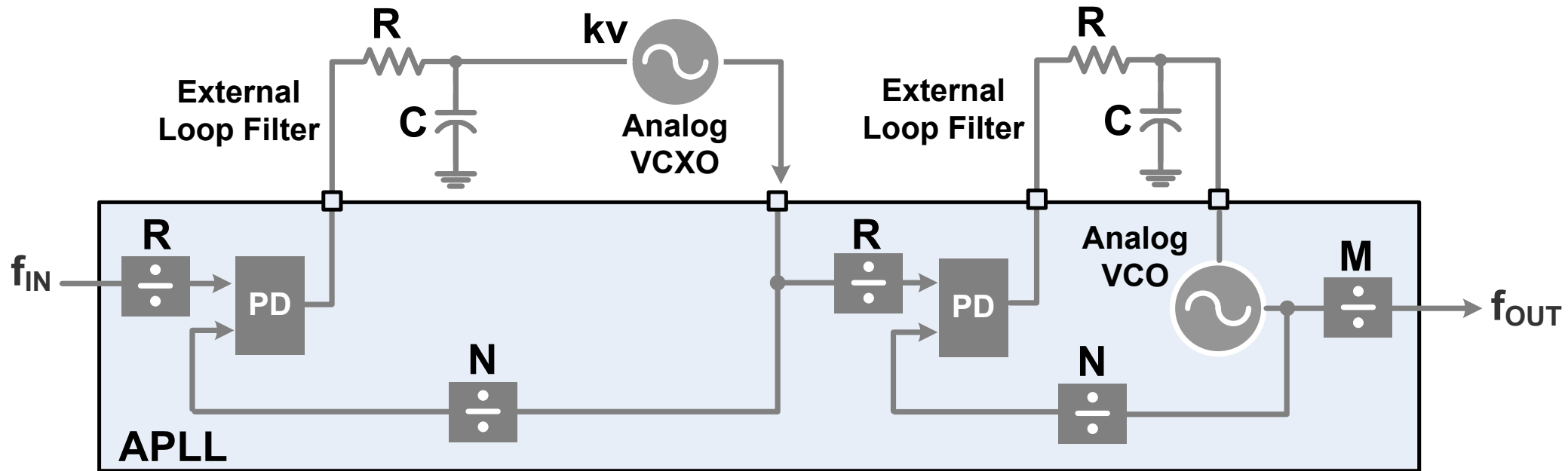


Two-Stage, Cascaded PLL Architecture

Legacy, Cascaded, Two-Stage PLL Architecture

This architecture uses a discrete, analog, narrowband VCXO-based PLL to implement jitter cleaning in its first stage. The VCXO must be used as the PLL's VCO to achieve low phase noise in conjunction with an external loop filter.

The 2nd stage PLL relies on an analog wideband PLL to provide integer clock multiplication. This requires an additional external loop filter.



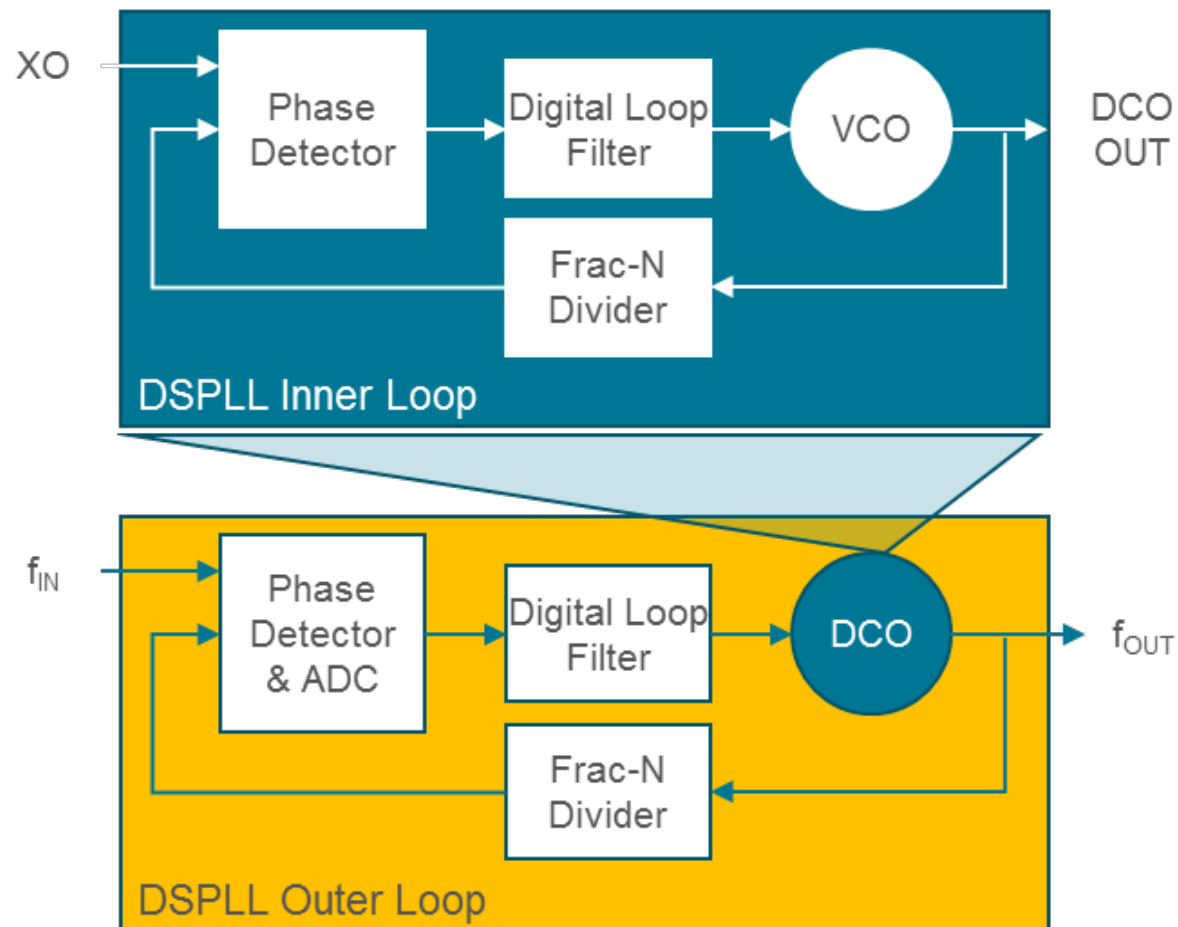
Two-Stage, Cascaded PLL Architecture

Pros and Cons of Cascaded, Two-Stage PLLs

Pros	Cons
✓ Low phase noise for integer-related frequencies to its input reference	✗ Multiple devices required to support non-integer-related frequencies
✓ Benefits and design requirements well understood by many designers	✗ Requires large footprint, discrete VCXOs, loop filters, LDOs
✓ Design drawbacks and guidelines also well understood by many designers	
	✗ High power
	✗ Large footprint
	✗ Each external node in the PLL is susceptible to noise
	✗ Susceptible to vibration

Pros and Cons of Two-Stage, Cascaded PLL Architectures

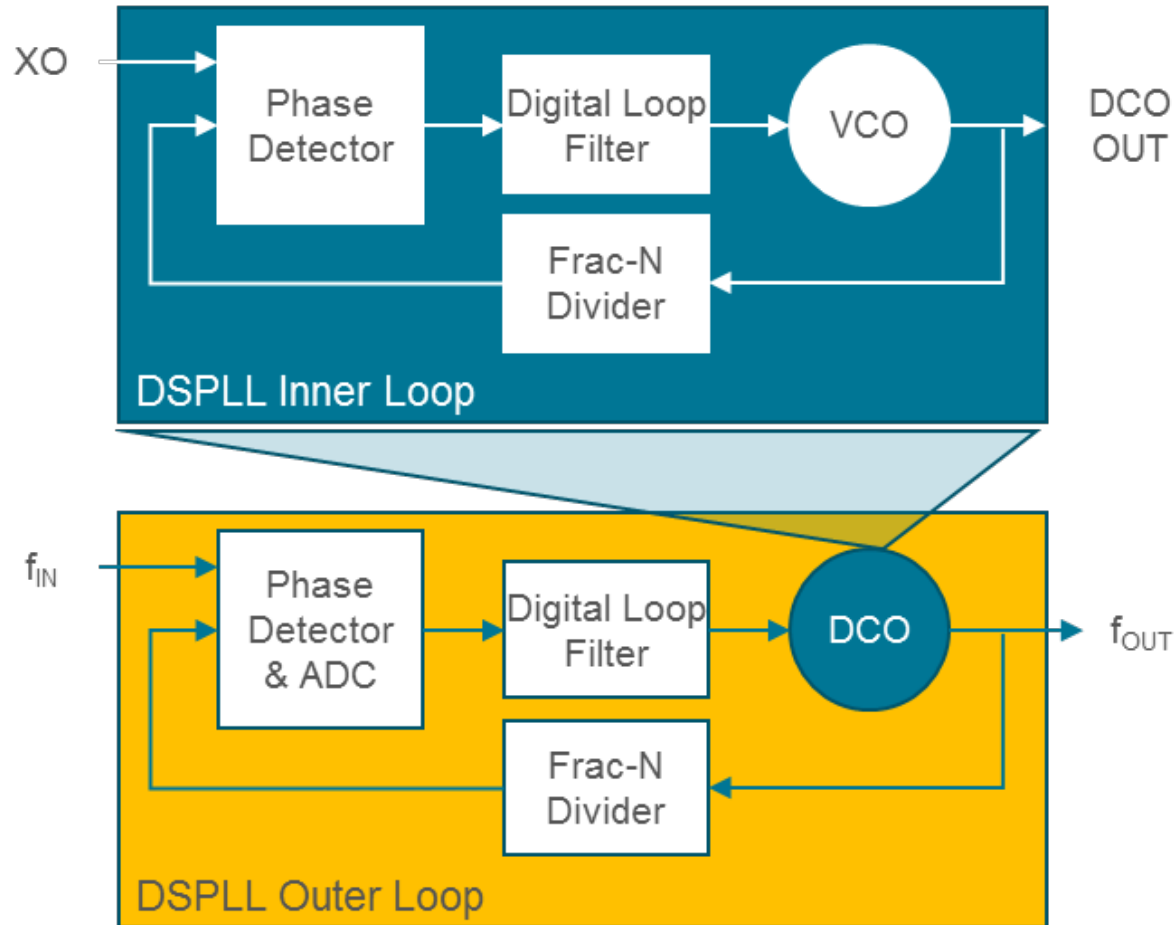
DSPLL Architecture Overview



Single-chip DSPLL Architecture

- The DSPLL architecture integrates and improves upon the traditional solution.
- DSPLL technology provides system clocks such as Ethernet and baseband...
- ...and the RF ultra-low phase noise clocks that **meet demanding 4G/LTE phase noise requirements with margin**.

DSPLL Architecture Explanation



Single-chip DSPLL Architecture

- The inner loop acts as a digitally-controlled oscillator for the outer loop, providing fractional clock synthesis with low phase noise without LC-oscillators and discrete VCXOs.
- The outer loop digitally tunes the operating frequency of the inner loop, synchronizes to external reference clocks, attenuates jitter, and generates clocks.
- All elements of the DSPLL are integrated on-chip, eliminating the need for discrete filter components and enabling easy PLL bandwidth adjustments to optimize phase noise performance.

Simplified Device Programming

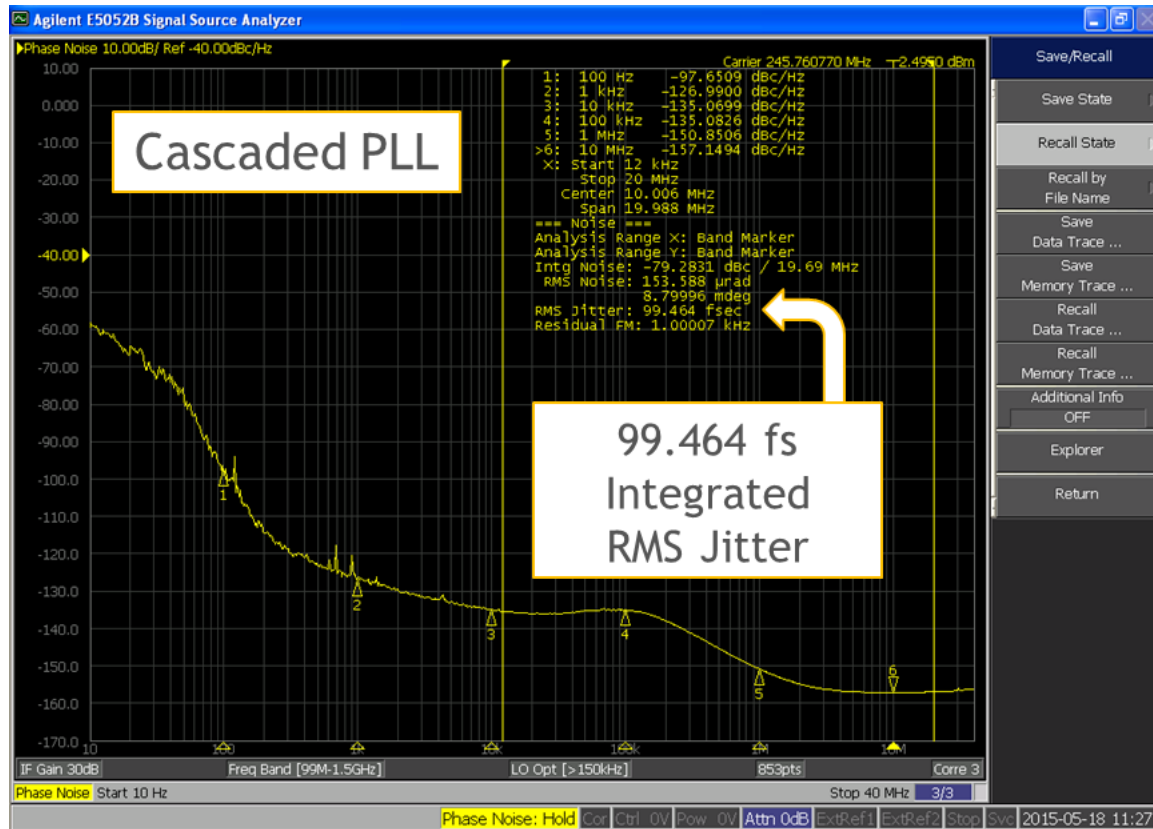


- Traditional cascaded PLL calculations and settings are done manually; a cumbersome, error-prone process.
- [ClockBuilder Pro](#) is a simple, easy to use software tool that customizes the DSPLL in minutes.
- Enter the input and output frequencies, set the DSPLL bandwidth and other operating parameters, and generate a device configuration.
- This allows simple, efficient testing, and speeds time to market.

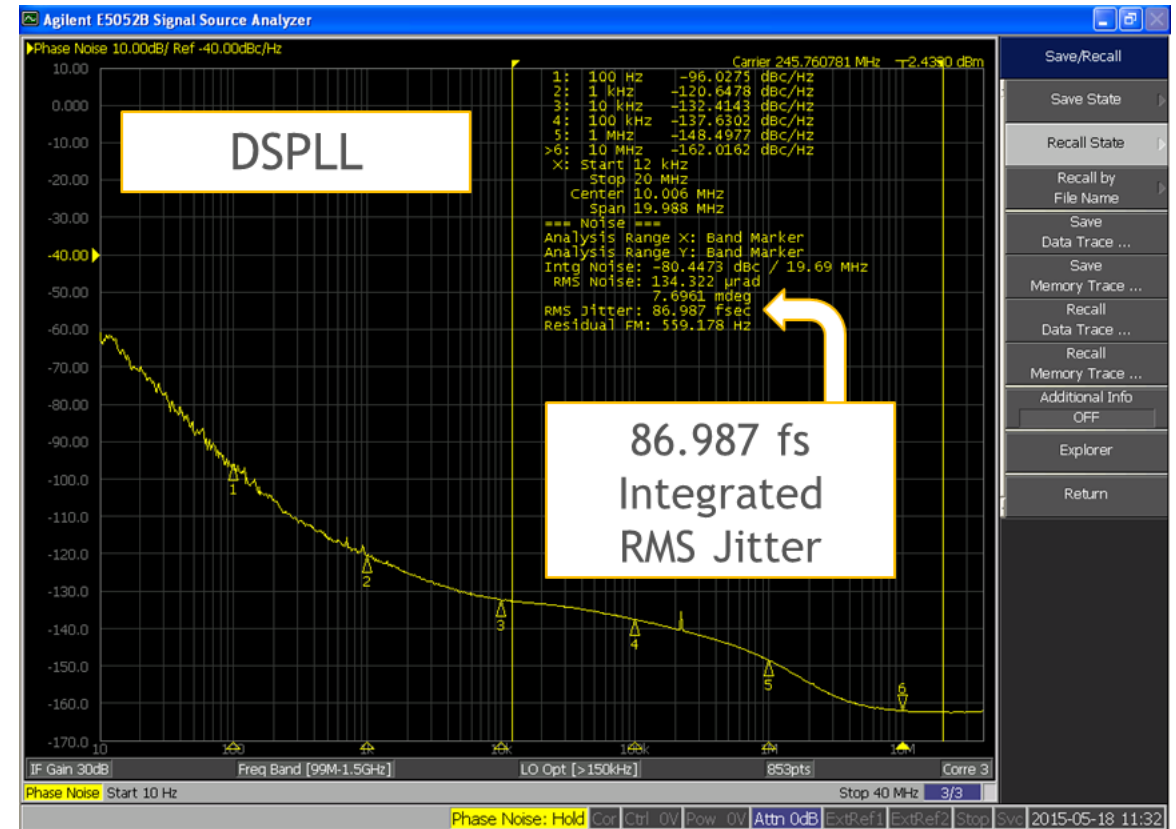
ClockBuilder Pro Software is Simple to Use

Performance: DSPLL vs. Cascaded, Two-Stage PLL

- DSPLL technology performance meets or exceeds that of traditional solutions.



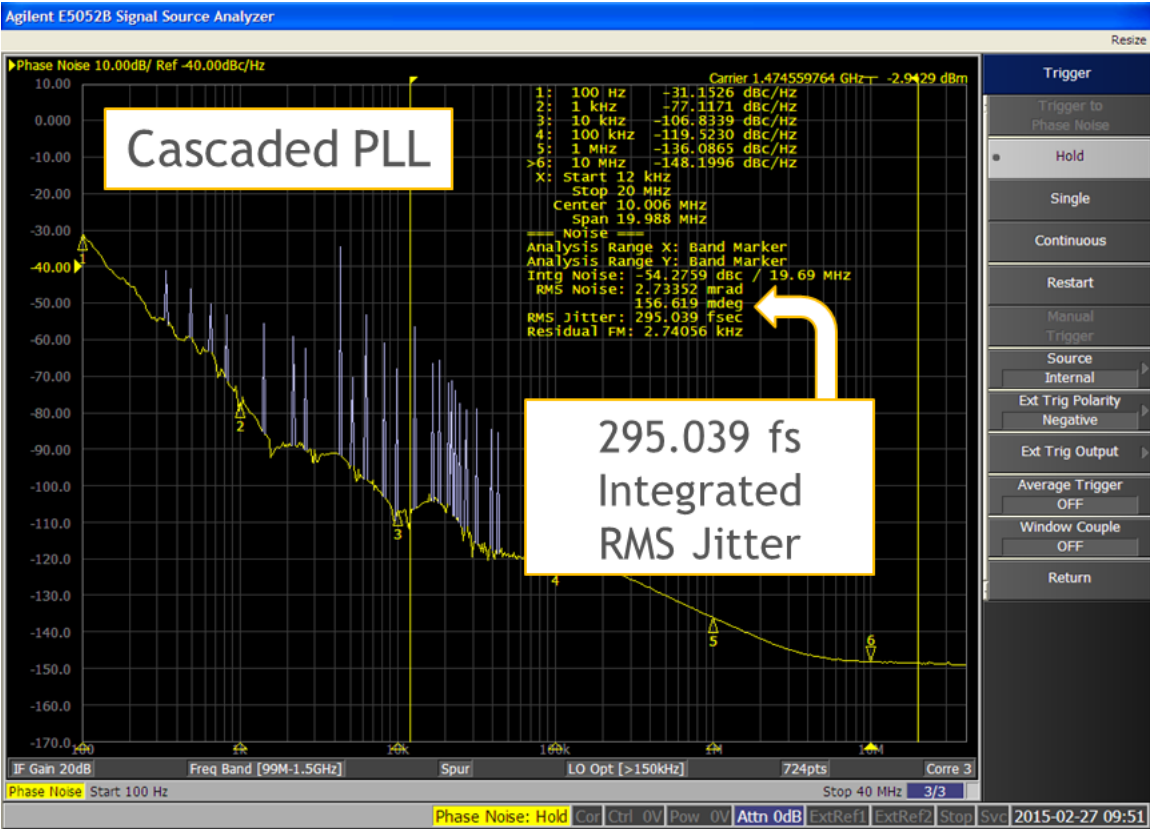
*Cascaded, Two-Stage PLL Performance
(245.76 MHz)*



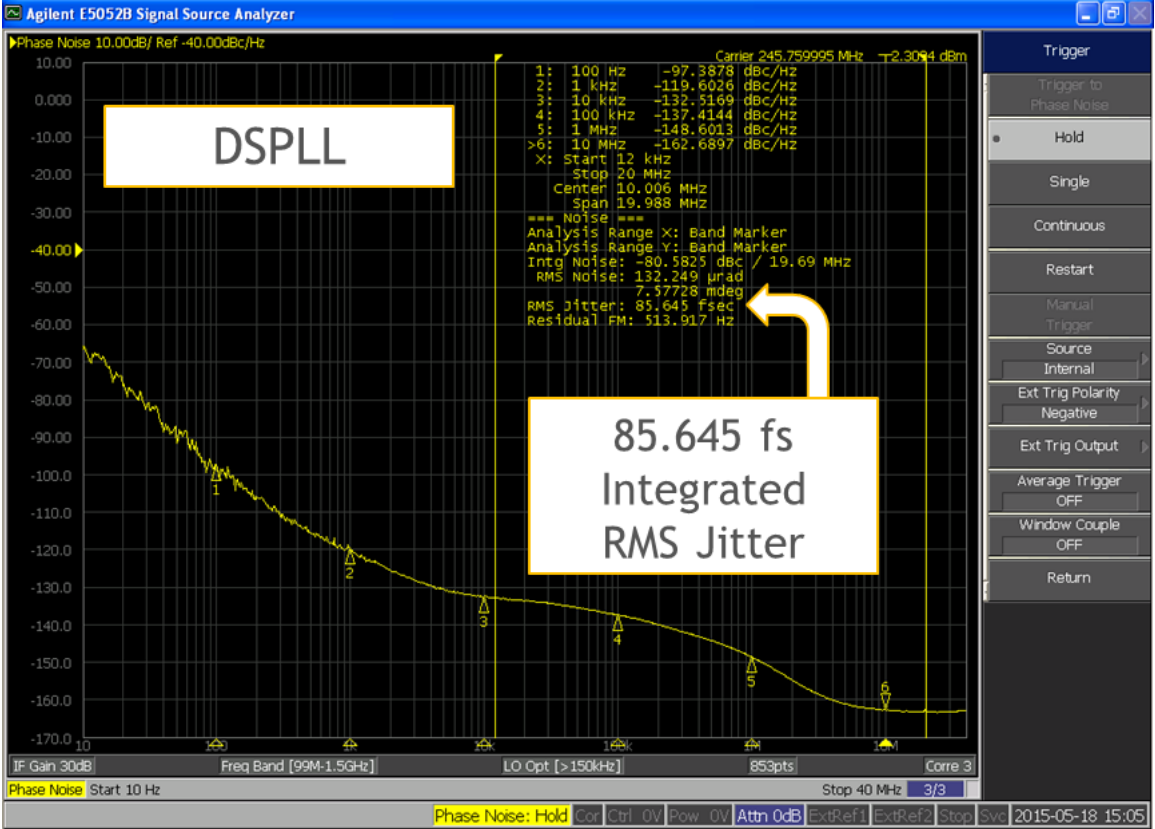
*DSPLL Performance
(245.76 MHz)*

DSPLL Immune to Vibration Effects

- RAN equipment is often deployed in external environments where wind, building or mechanical equipment can cause vibration. **DSPLL devices are highly immune to these effects.**



Cascaded, Two-Stage PLL Performance under Vibration



DSPLL Performance under Vibration

DSPLL is 66% Smaller than Cascaded, Two-stage PLL

	Cascaded PLL in mm ²	DSPLL in mm ²
DUT	81	81
VCXO	151.2	-
Crystal	-	8
Loop filters	9.3	-
Power supply filtering	22.8	3.7
Other	17.7	1.5
Total	282 mm²	94.3 mm²

DSPLL Footprint Comparison to Cascaded, Two-stage PLL

- The table shows component footprints and does not take into account PCB spacing or routing rules, further improving DSPLL's size advantage.
- DSPLL makes design easier, because it integrates sensitive, large components on-chip, including the VCXO and power supply filtering components.

DSPLL is 30% Lower Power than Cascaded, Two-stage PLL

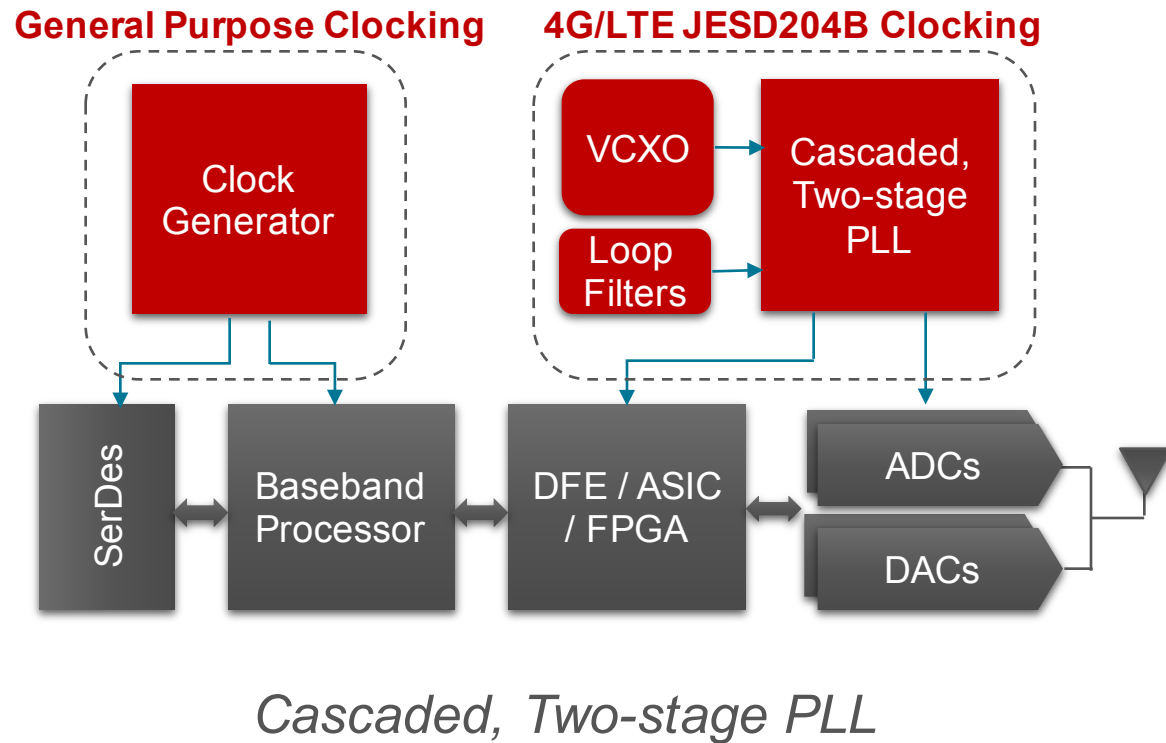
Description	Cascaded PLL	DSPLL
Supply Voltage	3.3V	3.3V analog + 1.8V core
Supply Current	600 mA	300 mA
Total Power	1.9 W	1.3 W

DSPLL Power Consumption Comparison to Cascaded, Two-stage PLL

- Improves RAN equipment design by reducing current consumption and heat in small enclosures.

Designs with Cascaded, Two-stage PLL

- RRH, small cell and DAS designs require a combination of **low-phase noise RF clocks plus baseband and Ethernet clocks**. These clock domains are **non-integer related**, forcing traditional solutions to use a cascaded, two-stage PLL and a discrete clock generator.



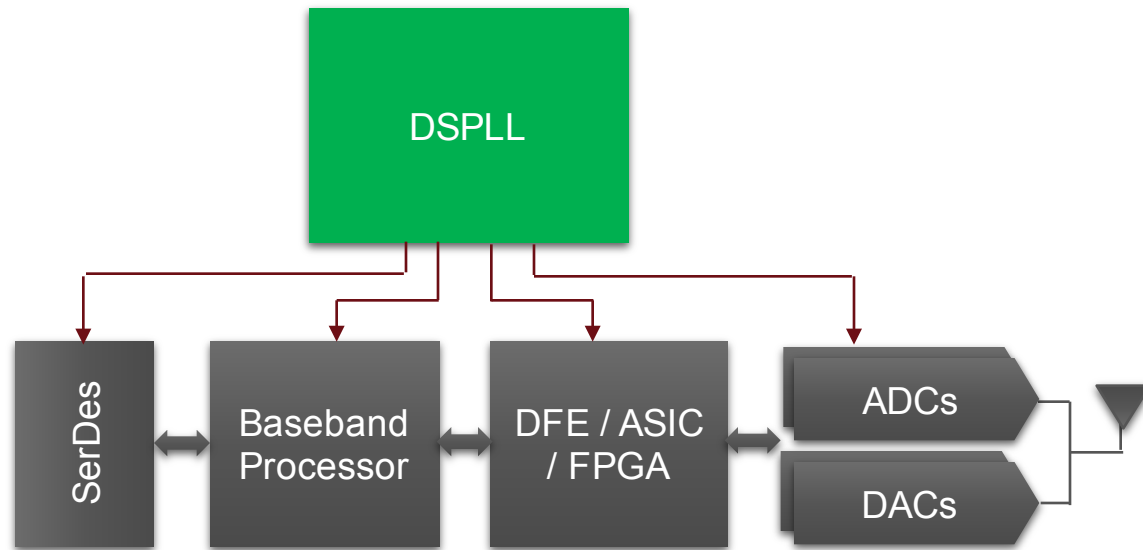
Cascaded, Two-stage PLL Design Details

- Two separate clock devices
 - Discrete clock for Ethernet and baseband timing
 - Cascaded, two-stage PLL provides RF timing
- External VCXO and loop filters required
- 339mm² PCB area
 - 282mm² for cascaded PLL + 57mm² for clock IC
- 2.4W power consumption
 - 1.9W for cascaded PLL + 0.5W for clock IC

Designs with DSPLL

- RRH, small cell and MDAS designs require a combination of **low-phase noise RF clocks plus baseband and Ethernet clocks**. These clock domains are **non-integer related**. This poses no problem for DSPLL.

General Purpose and 4G/LTE JESD204B Clocking

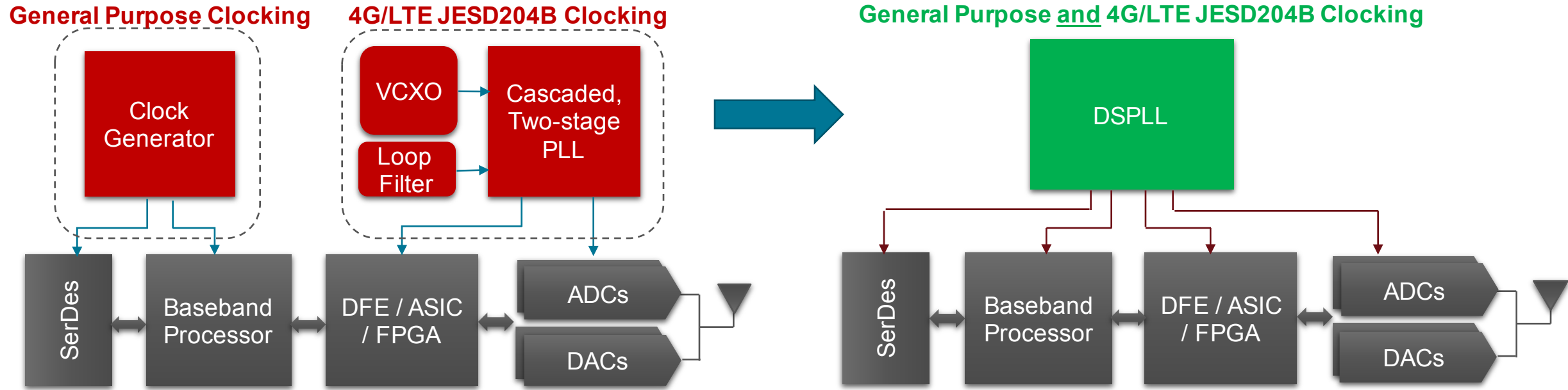


DSPLL Solution

DSPLL Design Details

- Single IC
 - All timing domains from a single IC with performance margin to spare
- No external VCXOs or loop filters
- 94mm² PCB area (75% smaller)
- 1.3W power consumption (50% lower power)

Smaller, Lower Power, Better, Faster to Market



- Silicon Labs' **proven** DSPLL technology **saves space, power, and cost**, and is **easier to design with**, speeding time to market.
- DSPLL **performs better** than legacy solutions.

[Click Here to Investigate DSPLL Si538x RAN solutions.](#)

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